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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.
09/167,502	01/06/98	RINCON MORA G	TI-28072

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EXAMINER	
CHOE,H	
ART UNIT	**PAPER NUMBER**
2817	4

DATE MAILED: 03/26/99

Please find below and/or attached an Office communication concerning this application or proceeding.

Commissioner of Patents and Trademarks

Office Action Summary	Application No. 09/167,506	Applicant(s) Rincon-Mora
	Examiner Henry Choe	Group Art Unit 2817

☐ Responsive to communication(s) filed on _____ .

☐ This action is **FINAL**.

☐ Since this application is in condition for allowance except for formal matters, **prosecution as to the merits is closed** in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11; 453 O.G. 213.

A shortened statutory period for response to this action is set to expire 3 month(s), or thirty days, whichever is longer, from the mailing date of this communication. Failure to respond within the period for response will cause the application to become abandoned. (35 U.S.C. § 133). Extensions of time may be obtained under the provisions of 37 CFR 1.136(a).

Disposition of Claims

☒ Claim(s) *1-9* is/are pending in the application.

Of the above, claim(s) _____ is/are withdrawn from consideration.

☐ Claim(s) _____ is/are allowed.

☒ Claim(s) *1-9* is/are rejected.

☐ Claim(s) _____ is/are objected to.

☐ Claims _____ are subject to restriction or election requirement.

Application Papers

☒ See the attached Notice of Draftsperson's Patent Drawing Review, PTO-948.

☐ The drawing(s) filed on _____ is/are objected to by the Examiner.

☐ The proposed drawing correction, filed on _____ is ☐approved ☐disapproved.

☒ The specification is objected to by the Examiner.

☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. § 119

☐ Acknowledgement is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d).

☐ All ☐ Some* ☐ None of the CERTIFIED copies of the priority documents have been

☐ received.

☐ received in Application No. (Series Code/Serial Number) _____ .

☐ received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

*Certified copies not received: _____ .

☐ Acknowledgement is made of a claim for domestic priority under 35 U.S.C. § 119(e).

Attachment(s)

☒ Notice of References Cited, PTO-892

☒ Information Disclosure Statement(s), PTO-1449, Paper No(s). 5

☐ Interview Summary, PTO-413

☒ Notice of Draftsperson's Patent Drawing Review, PTO-948

☐ Notice of Informal Patent Application, PTO-152

--- SEE OFFICE ACTION ON THE FOLLOWING PAGES ---

DETAILED ACTION

Specification

1. The disclosure is objected to because of the following informalities: In the brief description of the drawings, Fig.4 is not mentioned. Fig. 4 should be Fig.5. Fig. 5 should be Fig. 6 . Appropriate correction is required.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless --
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-9 are rejected under 35 U.S.C. 102(b) as being anticipated by Schade Jr. Schade discloses an operational amplifier for amplifying an input signal (IN and NOT IN) applied to an input node (Gate node of Q1 or Q2) to provide an output signal (OUT) at an amplifier output node (N2) comprising a first amplifier stage (Q1, Q2, Q31 and Q32) having an internal node (COMP) as an input thereto and having a first stage output node (11) wherein the first amplifier stage (Q1, Q2, Q31, Q32) having a bipolar transistor current mirror (Q31 and Q32) and a diode connected transistor (Q31) and a ratioed transistor connected together forming a current mirror (Q31 and Q32) and wherein the diode connected transistor (Q31) senses the

capacitive current (ic) at the internal node (COMP) and the ratioed transistor amplifies the capacitive current (ic) and the capacitive current (ic) flows through the capacitor (C) and the capacitive current (ic) is inherently sensed at the internal node (COMP) and inherently amplified by the first amplifier stage (Q1, Q2, Q31 and Q32), a second amplifier stage (Q11 and Q12) connected to the first amplifier stage (Q1, Q2, Q31 and Q32) having the input node (Gate node of Q1 or Q2) as an input thereto and providing the output signal (OUT) at the amplifier output node (N2) wherein the second amplifier stage (Q11 and Q12) is connected to the first amplifier stage (Q1, Q2, Q31 and Q32) such that the first stage output node (11) is common with the amplifier output node (N2) and is connected to the first amplifier stage (Q1, Q2, Q31 and Q32) such that the first stage output node (11) is connected to the input node (Gate node of Q1 or Q2), a third amplifier stage (Q21 and Q22) having a third stage input node (21) connected to the first stage output node (11) through the Q21 and Q11 and to the second stage output node (12) and providing the output signal (OUT) at the amplifier output node (N2), and a capacitor (C) connected between the amplifier output node (N2) and the internal node (COMP) wherein the capacitor (C) is connected such that a left-hand-plane zero is inherently provided in the compensated amplifier and the left-hand-plane zero is inherently selected so as to optimize compensation for the compensated amplifier.

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Henry Choe whose telephone number is (703) 305-0576.

Robert Pascal
Supervisory Patent Examiner
Technology Center 2800